Application No.: 10/092,064
Filed: March 5, 2002
TC Art Unit: 2664
Confirmation No.: 7833

REMARKS

The instant Remarks are filed in response to the official action dated November 15, 2005. Reconsideration is respectfully requested.

The status of the claims is as follows:

Claims 1-10 are currently pending.

Claims 1-6 stand rejected.

Claims 7-10 are allowable.

The Examiner has rejected claims 1-6 under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 6,078,733 to Osborne (the Osborne reference). The Applicant respectfully submits, however, that base claim 1 and claims 2-6 dependent therefrom recite non-obvious subject matter that distinguishes over the art of record.

For example, claim 1 recites a link layer device having at least one unique identifier associated therewith, including an input data line (301) for receiving a plurality of data packets, an output data line (305), a data receiver (302) coupled to the input data line (301), a channel mapper (308) coupled to the data receiver (302), a received data FIFO (312) coupled to the channel mapper (308), a feed-forward data FIFO (306) coupled to the channel mapper (308), a transmitter data FIFO (310), and a data transmitter (304) (see Fig. 3 of the application). As recited in

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claim 1, the channel mapper is operative to receive the plurality of received data packets, to divert the received data packets having a destination identifier equivalent to the unique destination identifier associated with the link layer device to the received data FIFO, and to divert the remaining data packets of the plurality of received data packets to the feed-forward data FIFO. As further recited in claim 1, the transmitter data FIFO contains a plurality of data packets to be transmitted, in which each of the plurality of data packets to be transmitted has a destination identifier and a plurality of data. The data transmitter, which has an output coupled to the output data line and inputs coupled to the feed-forward data FIFO and the transmitter data FIFO, is configured to retrieve data packets from the feed-forward data FIFO and the transmitter data FIFO, and to transmit the retrieved data packets over the output data line, as recited in claim 1. As described in the instant application, the received data packets diverted by the channel mapper (308) to the received data FIFO (312) are ultimately provided to input/output ports (315) via an egress data processor (316) (see page 12, line 28, to page 13, line 3, and Fig. 3, of the application).

The official action indicates that the Osborne reference teaches a link layer device that includes a data receiver (the

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receive side 82 of a network interface), a channel mapper (the mapping circuit 164), a received data FIFO (the input FIFO 160), a feed-forward data FIFO (the DMA circuit 154), a transmitter data FIFO, and a data transmitter (see Figs. 3, 5, and 9 of Osborne). The official action further indicates that the mapping circuit (164) is operative to receive a plurality of data packets, to divert the received data packets having a destination identifier equivalent to the unique destination identifier of the link layer device to the input FIFO (160), and to divert the remaining plurality of received data packets to the DMA circuit (154) (see Fig. 5 of Osborne). The Applicant respectfully submits, however, that the Osborne reference neither teaches nor suggests a link layer device having the structure and functionality recited in claim 1.

For example, as shown in Fig. 5 of the Osborne reference, the mapping circuit (164) is contained within the receive side (82) of the network interface. Contrary to what is indicated in the official action, the mapping circuit (164) does not divert received data packets having a destination identifier equivalent to the unique destination identifier of a link layer device to the input FIFO (160), nor does it divert the remaining plurality of received data packets to the DMA circuit (154). Instead, as

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illustrated in Fig. 5 of the Osborne reference, the mapping circuit (164) receives virtual addresses from a multiplexor (163), maps the virtual addresses to physical addresses, and provides the physical addresses to the output FIFO (156). As best understood, the mapping circuit (164) also provides address information directly to the DMA circuit (154) (see Fig. 5 of Osborne).

Significantly, the mapping circuit (164) provides no information whatsoever, *i.e.*, neither data nor address information, to the input FIFO (160) (see Fig. 5 of Osborne). The Applicant therefore respectfully submits that the mapping circuit (164) of the Osborne reference does not correspond to the channel mapper of claim 1, which receives a plurality of data packets, diverts the received data packets having a destination identifier equivalent to the unique destination identifier of the link layer device to a received data FIFO, and diverts the remaining plurality of received data packets to a feed-forward data FIFO, as recited in claim 1. As shown in Fig. 5 of the Osborne reference, the input FIFO (160) receives data only from the network – the input FIFO (160) receives no data or any other type of information from the mapping circuit (164).

As mentioned above, the Osborne reference discloses that the mapping circuit (164) receives virtual addresses from the

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multiplexor (163), maps the virtual addresses to physical addresses, and provides address information to both the output FIFO (156) and the DMA circuit (154) (see Fig. 5 of Osborne). Accordingly, as disclosed by Osborne, the mapping circuit (164) is configured to divert address information to the output FIFO (156) and the DMA circuit (154).

The Applicant respectfully points out that even if the output FIFO (156) disclosed in the Osborne reference were deemed to correspond to the received data FIFO of claim 1, the Osborne reference still would neither teach nor suggest a link layer device having the structure and functionality recited in claim 1. This is because the output FIFO (156) merely receives physical addresses from the mapping circuit (164), and provides data and address information to the DMA circuit (154), which processes the data for subsequent transmission over an output line to the host computer (see Fig. 5 of Osborne). In effect, the output FIFO (156) and the DMA circuit (154) provide data to the same destination, namely, the host computer, via an output line.

In contrast, as recited in claim 1, the channel mapper diverts received data packets having a destination identifier equivalent to the unique destination identifier associated with the link layer device to the received data FIFO, and diverts the

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FAX. (617) 451-0313

remaining data packets of the plurality of received data packets to the feed-forward data FIFO. As explained above, the data provided to the received data FIFO (312) and the feed-forward data FIFO (306) by the channel mapper (308) are ultimately provided to two different destinations via the input/output ports (315) and the output data line (305), respectively (see Fig. 3 of the application). Accordingly, the mapping circuit (164) disclosed in the Osborne reference does not correspond to the channel mapper of claim 1. Further, neither the input FIFO (160) nor the output FIFO (156) disclosed by Osborne corresponds to the received data FIFO of claim 1.

By providing a link layer device including a channel mapper that can divert received data packets having a destination identifier equivalent to the unique destination identifier associated with the link layer device to a received data FIFO, while diverting the remaining data packets of the plurality of received data packets to a feed-forward data FIFO, as recited in claim 1, a plurality of such link layer devices can be interconnected in a serial daisy chain fashion (see page 9, lines 6-8, and Fig. 2, of the application). Because the network interface disclosed in the Osborne reference does not include the channel mapper of claim 1, a plurality of such network interfaces

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FAX. (617) 451-0313

cannot be similarly interconnected in a serial daisy chain fashion.

Because the Osborne reference neither teaches nor suggests a link layer device that includes a channel mapper operative to receive a plurality of received data packets, to divert the received data packets having a destination identifier equivalent to the unique destination identifier associated with the link layer device to a received data FIFO, and to divert the remaining data packets of the plurality of received data packets to a feed-forward data FIFO, as recited in base claim 1, the Applicant respectfully submits that the Osborne reference does not anticipate claim 1 and claims 2-6 dependent therefrom. Accordingly, it is respectfully submitted that the rejections of claims 1-6 under 35 U.S.C. 102 are unwarranted and should be withdrawn.

In view of the foregoing, it is respectfully submitted that the present application is in a condition for allowance. Early and favorable action is respectfully requested.

The Examiner is encouraged to telephone the undersigned Attorney to discuss any matter that would expedite allowance of

WEINGARTEN, SCHURGIN,
GAGNEBIN & LEBOVICI LLP
TEL. (617) 542-2290
FAX. (617) 451-0313

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the present application.

Respectfully submitted,

MICHAEL D. SCHOLTEN

By _____
Richard E. Gamache
Registration No. 39,196
Attorney for Applicant

WEINGARTEN, SCHURGIN,
GAGNEBIN & LEBOVICI LLP
Ten Post Office Square
Boston, MA 02109
Telephone: (617) 542-2290
Telecopier: (617) 451-0313

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WEINGARTEN, SCHURGIN,
GAGNEBIN & LEBOVICI LLP
TEL. (617) 542-2290
FAX. (617) 451-0313